深 圳 市 艾 斯 迪 科 技 有 限 公 司

LCDGO TECHNOLOGY Co.,Ltd

7.0 寸 LCD 模组规格书

SPECIFCATION

承 认 印 Approved by	
审核：	确认：

客户确认结果：

Customer
客　　户：_____

Product
品　　名：7.0 寸 LCD 模组

Part NO.
产品料号：LCDT701280M31

DATE
日　　期：2019/10/14

Approved 核　准	Checked 审　核	Prepared 制　作

Contents

Document Revision History

Change No.	Date	Subject And Reason	Version No.	Responser
1	2019.10.14	New	01	ZW

1.0 General Description

1.1 Introduction

LCDT701280M31 color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel and a driving circuit. This TFT LCD has a 7.0 (9:16) inch diagonally measured active display area with (800 horizontal by 1280 vertical pixel) resolution.

1.2. Features

7.0(9:16 diagonal) inch configuration
Image Reversion: UP/DOWN and LEFT/RIGHT
ROHS design

1.3. General information

Item	Specification	Unit
Outline Dimension	99.8(H) x 161.05V) x2.65 (D)	mm
Display area	94.2(H) x 150.72 (V)	mm
Number of Pixel	800(H) x3(RGB)x 1280 (V)	pixels
Pixel pitch	0.11775(H) x3(RGB)x 0.11775 (V)	mm
Pixel arrangement	RGB Vertical stripe	
Display mode	IPS(Normal Black)	
Color Filter Array	RGB vertical stripes	
Luminous	300(TYP)	cd/m^2
Weight	TBD	g
Interface	MIPI	

2.0 Interface pin define:

Pin No.	Symbol	I/O		
1	LEDA	Power for LED backlight (Anode)		
2	LEDA	Power for LED backlight (Anode)		
3	LEDA	Power for LED backlight (Anode)		
4	NC	No connect.		
5	LEDK	Power for LED backlight (Cathode)		
6	LEDK	Power for LED backlight (Cathode)		
7	LEDK	Power for LED backlight (Cathode)		
8	LEDK	Power for LED backlight (Cathode)		
9	GND	Ground		
10	GND	Ground		
11	MIPI_D2+	HSSI_D2_Pare differential small amplitude signals.		
12	MIPI_D2-	HSSI_D2_Nare differential small amplitude signals.		
13	GND	Ground		
14	MIPI_D1+	HSSI_D1_Pare differential small amplitude signals.		
15	MIPI_D1-	HSSI_D1_Nare differential small amplitude signals.		
16	GND	Ground.		
17	MIPI_CLK+	HSSI_CLK_P are differential small amplitude signals		
18	MIPI_CLK-	HSSI_CLK_N are differential small amplitude signals		
19	GND	Ground.		
20	MIPI_D0+	HSSI_D0_P are differential small amplitude signals.		
21	MIPI_D0-	HSSI_D0_N are differential small amplitude signals.		
22	GND	Ground.		
23	MIPI_D3+	HSSI_D3_P are differential small amplitude signals.		
24	MIPI_D3-	HSSI_D3_N are differential small amplitude signals.		
25	GND	Ground.		
26	NC			
27	**RESET**	**Reset signal**		
28	NC			
29	**VDD1V8**	**I/O power supply**		
30	VDD3V3	Power supper 3.0-3.6 V		
31	VDD3V3	Power supper 3.0-3.6 V		

3. Operation Specifications

3.1 Absolute Maximum Ratings

Electrical Maximum Ratings (VSS=0V)

Table 1: Electrical Maximum Ratings – for IC

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage	VCC	-0.3	+3.6	V	GND=0
	IOVCC	+0.3	+3.6	V	GND=0

Note:

1. VCC,IOVCC, GND must be maintained.

2. The modules may be destroyed if they are used beyond the absolute maximum ratings.

3.Ta=25+/-2℃

3.2. Electrical Specifications(Typical Operation Conditions, At Ta = 25 °C)

Table 2

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Power Supply Voltage	VCC	3.0	3.3	3.6	V	-
	IOVCC	1.7	1.8	2.0	V	-

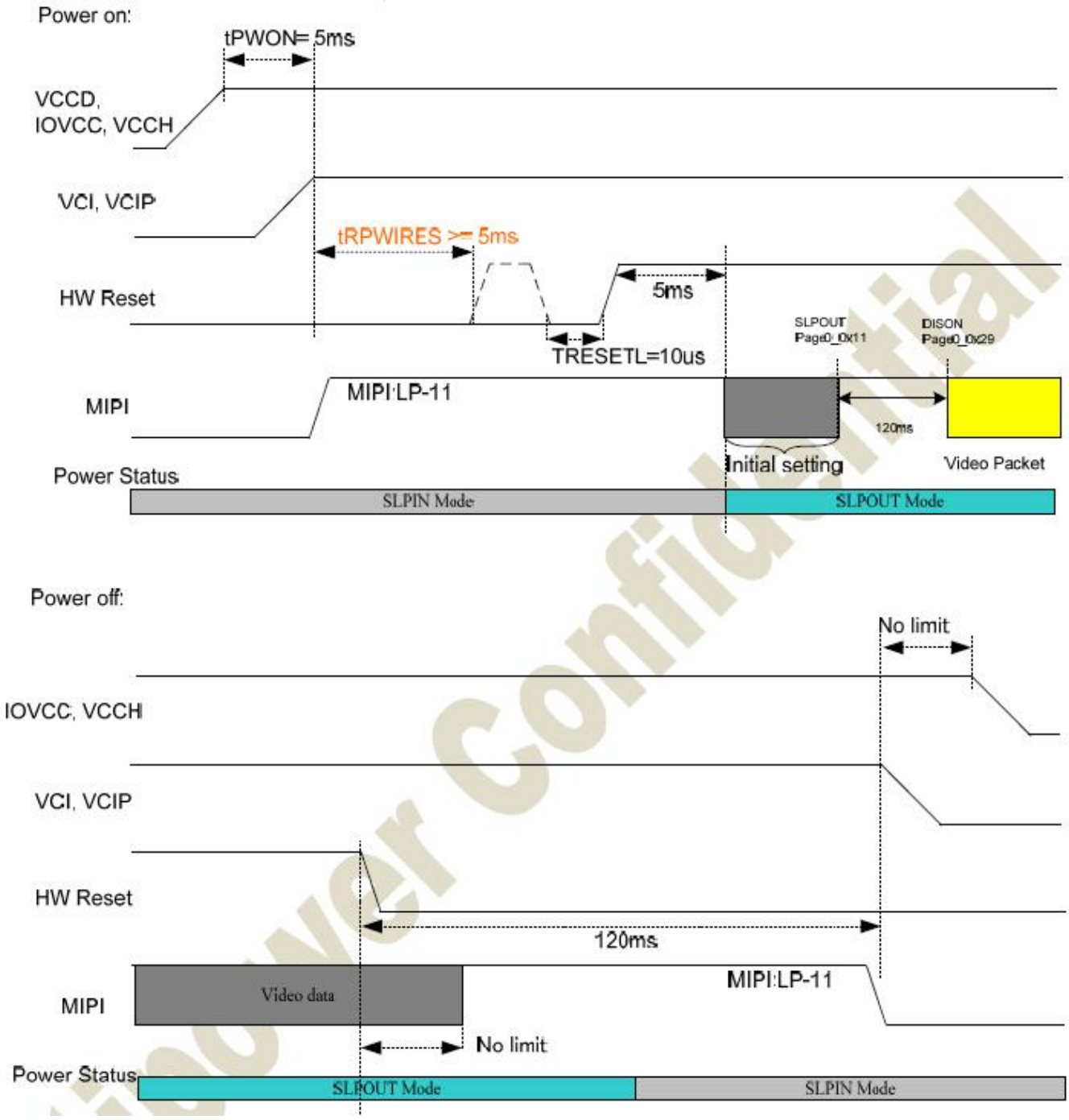
3.3 Back-light Unit:

PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
LED Current	IF	–	80	–	mA		–
Luminous	--	250	300		cd/m^2	IF=80mA	–
LED Voltage	VF	15	16	17.5	V	IF=80mA	–
Life Time		–	20000	–	Hr.	I≦80mA	
Color	White						

Note (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IF =80mA. The LED lifetime could be decreased if operating IF is larger than=80mA.

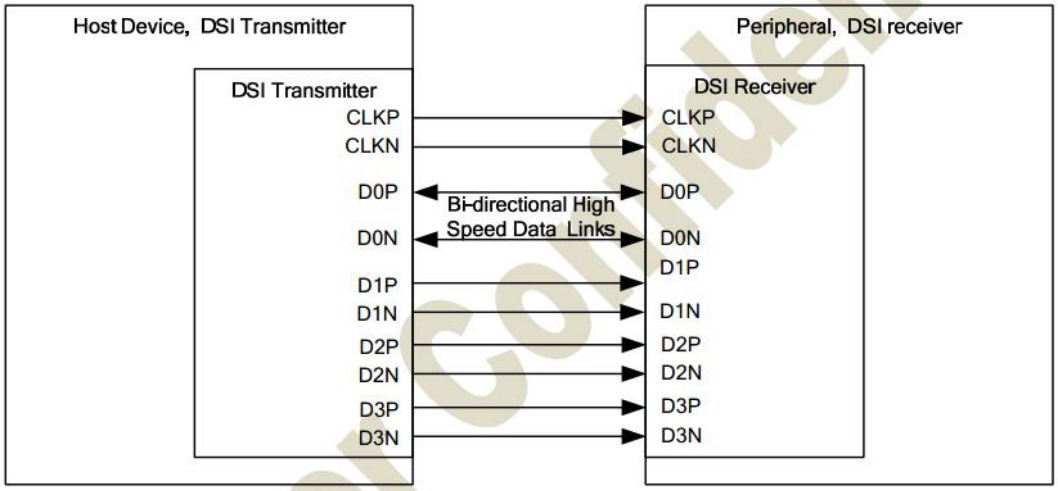
3.4 Power Sequence



3.4 MIPI Interface(Mobile Industry Processing Interface)

The Display Serial Interface (DSI) specifies the interface between a host processor and a peripheral. DSI builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-2 and DCS standards.

Figure 7.1 shows a simplified DSI interface. DSI sends display data or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals.



3.5 MIPI Signal Timing Characteristics

3.5.1 AC Electrical Characteristics

High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times.

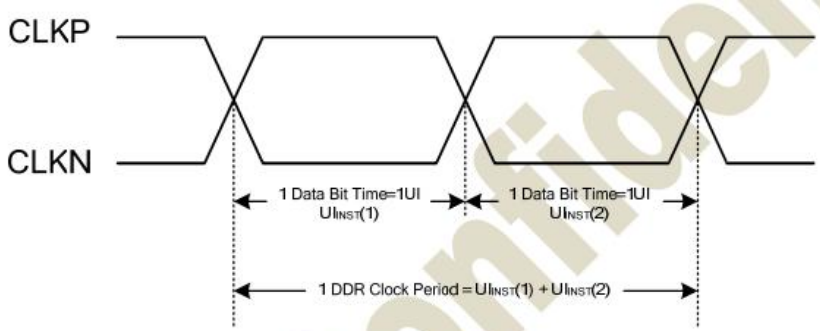


Figure 11.5: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI. The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3), (4), (5), (6)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 850bps of 1 data lane 24-bit data format/ 630Mbps of 1 data lane 18-bit data format/ 560Mbps of 1 data lane 16-bit data format.
(4) Maximum total bit rate is 1.7Gbps of 2 data lanes 24-bit data format/ 1.27Gbps of 2 data lane 18-bit data format/ 1.13Gbps of 2 data lane 16-bit data format.
(5) Maximum total bit rate is 2Gbps of 3 data lanes 24-bit data format/ 1.5Gbps of 3 data lane 18-bit data format/ 1.33Gbps of 3 data lane 16-bit data format.
(6) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

Table 11.11: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.13. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data. The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

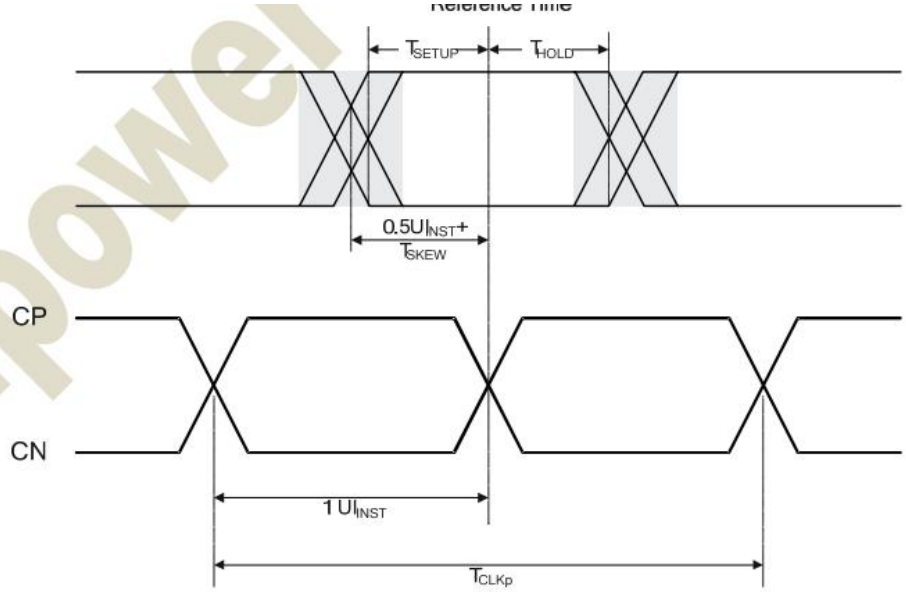


Figure 11.6: Data to Clock Timing Definitions

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 13.12. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 13.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

Table 11.12: Data to Clock Timing Specifications

Burst Mode Data Transmission

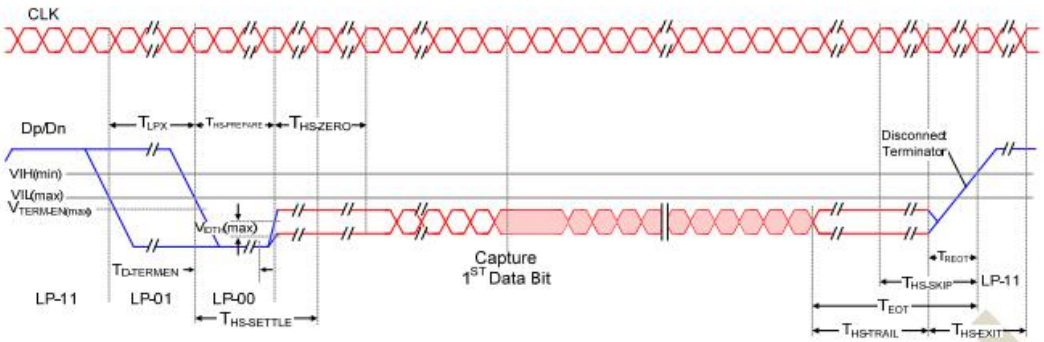


Figure 11.7: High-Speed Data Transmission in Bursts

Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

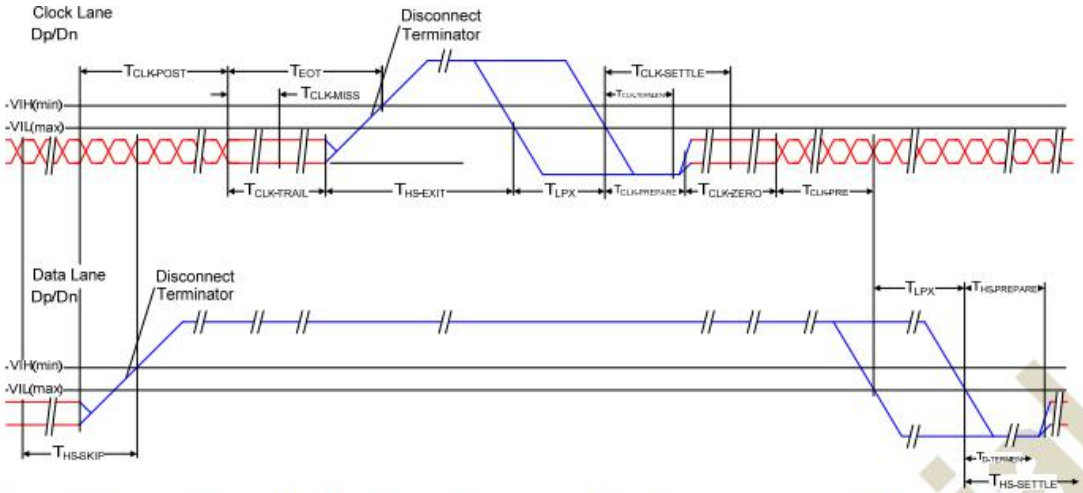


Figure 11.8: Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

3.5.2 Timing for MIPI Characteristics.

Horizontal Timings

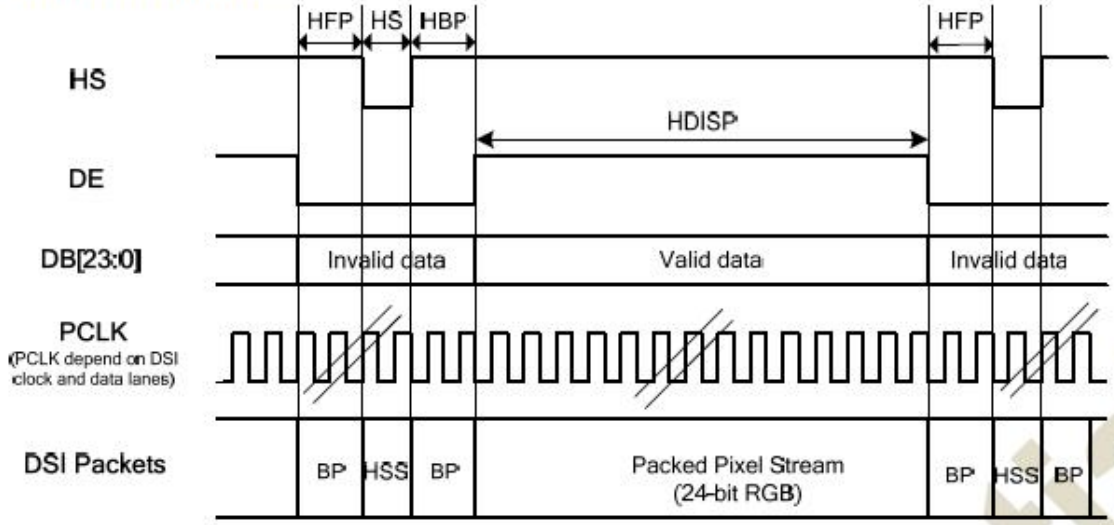


Figure 11.10: Horizontal Timing for DSI Video mode I/F

Resolution=800x1280 (T_A=25°C, IOVCC=1.8V, VCIP=VCI=VCCH=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	18	78	DCK
Horizontal back porch	HBP	-	5	18	78	DCK
Horizontal front porch	HFP	-	5	18	78	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	54 (Note1)	88	DCK
Horizontal active area	HDISP	-	-	800	-	DCK
Pixel Clock	PCLK	-	63.06 (Note2)	67.33 (Note2)	81.51 (Note2)	MHz

Note 1: HS+HBP > 0.5us.
Note 2: Pixel Clock = (HBLK+HDISP) * (VBK+VDISP) * Frame rate, Frame rate=60Hz.

Vertical Timings

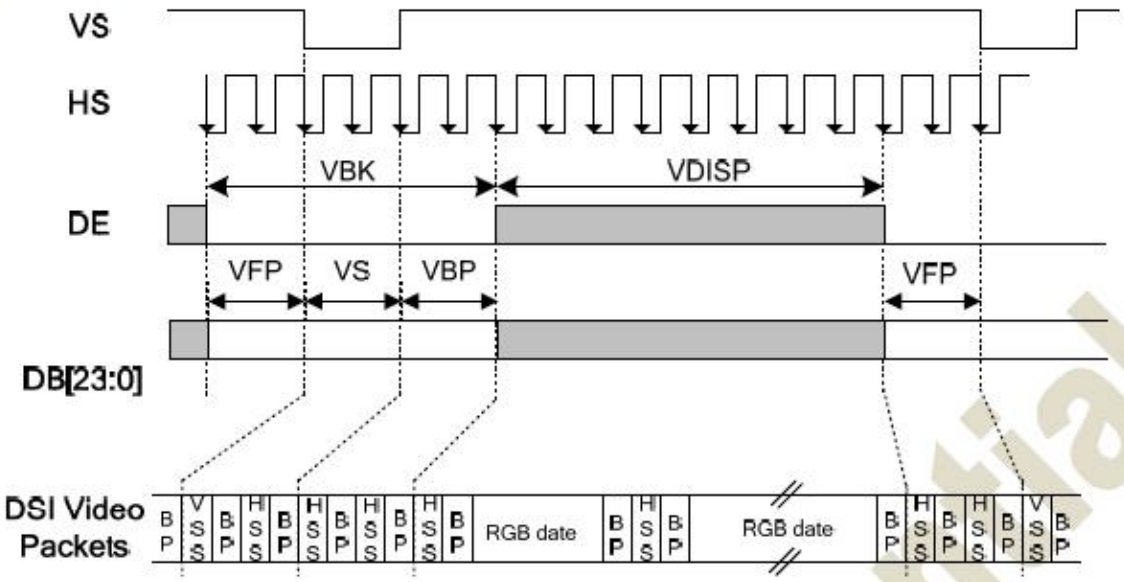


Figure 11.9: Vertical Timings for DPI I/F

Resolution=800x1280(T_A=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	4	200 Note(1)	Line
Vertical front porch	VFP	-	4	20	200	Line
Vertical back porch	VBP	-	2	10	200 Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	8	34	250	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

Resolution=720x1280 (TA=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	18	78	DCK
Horizontal back porch	HBP	-	5	18	78	DCK
Horizontal front porch	HFP	-	5	18	78	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	54 (Note1)	88	DCK
Horizontal active area	HDISP	-	-	720	-	DCK
			56.88 (Note2)	61.02 (Note2)	74.17 (Note2)	MHz

Note 1: HS+HBP > 0.5us.
Note 2: Pixel Clock = (HBLK+HDISP) * (VBK+VDISP) * Frame rate, Frame rate=60Hz.

4.0 Optical specification

(Taransmittance, contrast ratio, response time, viewing angle results are using CPT LC(Vlc=5V) + CPT Polarizer + Corresponding Backlight, reference only)

Ambient condition：25 ± 2°C，60 ± 10% RH，under 10 Lunx in the darkroom

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Transmittance		T	$\theta = \phi = 0°$	3.8	4.25	--	%	Note *1) *5) BASE ON CPT BL
Contrast Ratio		CR	---	600	800	---	---	Note *2)
Response Time		Tr+Tf	$\theta = \phi = 0°$	---	30	40	ms	Note *4)
Viewing angle	Vertical	U	CR≧10	--	85	--	degree	Note *3)
		D		--	85	--	degree	
	Horizontal	L		--	85	--	degree	
		R		--	85	--	degree	
Color Filter Chromacicity	W	x	$\theta = \phi = 0°$	0.270	0.300	0.330	---	Note *6) BASE ON CPT BL
		y		0.290	0.320	0.350	---	
	R	x		TBD	TBD	TBD	---	
		y		TBD	TBD	TBD	---	
	G	x		TBD	TBD	TBD	---	
		y		TBD	TBD	TBD	---	
	B	x		TBD	TBD	TBD	---	
		y		TBD	TBD	TBD	---	
	NTSC		CIE_1931	65	70	--	%	

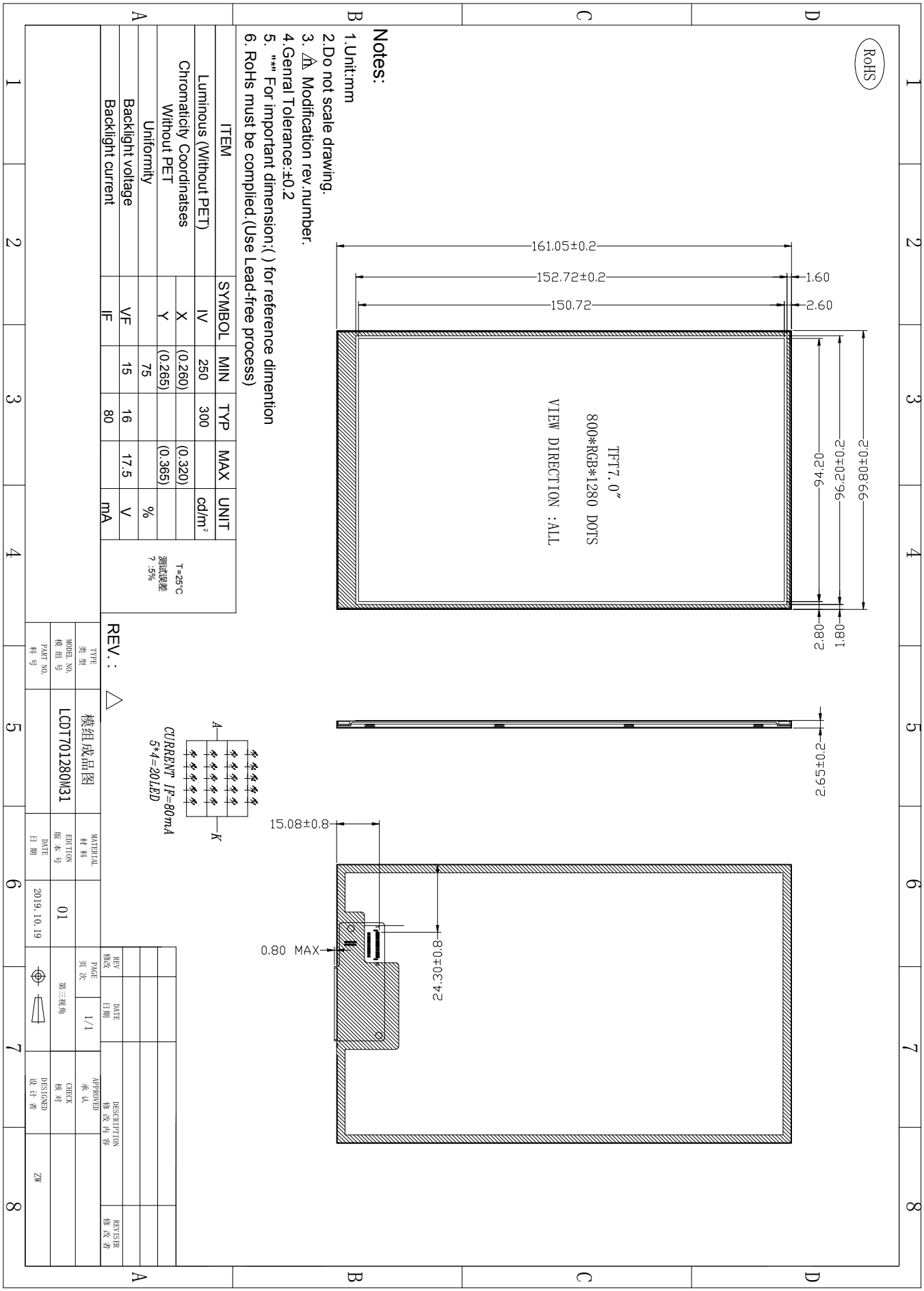
5.0 Reliability test items

NO	Item	Conditions	Remark
1	High Temperature Storage	Ta=+60℃,48hrs	
2	Low Temperature Storage	Ta=-20℃,48hrs	
3	High Temperature Operation	Ta=+50℃,48hrs	
4	Low Temperature Operation	Ta=-10℃,48hrs	
5	High Temperature and High Humidity (operation)	Ta=+50℃,80%RH,96hrs	
6	Thermal Cycling Test (non operation)	-20℃(0.5hr)→+60℃(0.5hr),100cycles	

Note: All tests above are practiced at module type.

There is no display function NG issue occurred, All the cosmetic specification is judged before the reliability stress.

6.0 Outline dimension



7.0 General Precaution

7.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

7.2 Asembly Precaytton

7.2.1 Please use the mounting hole on the module side in installing and do not bending or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.
7.2.2 Please design display housing in accordance with the following guide lines.
7.2.2.1 Housing case must be destined carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.
7.2.2.2 Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. The clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.
7.2.3 Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film, surface of LCD panel is easy to be flawed.)
7.2.4 Please do not press any parts on the rear side such as source IC, gate IC, and FPC during handling LCD module. If pressing rear part is unavoidable, handle the LCD module with care not to damage them.
7.2.5 Please wipe out LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.
7.2.6 Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.
7.2.7 Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.

7.3 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HannStar does not warrant the module, if customers disassemble or modify the module.

7.4 Breakage of LCD Panel

7.4.1 If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.
7.4.2 If liquid crystal contacts mouth or eyes, rinse out with water immediately.
7.4.3 If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.
7.4.4 Handle carefully with chips of glass that may cause injury, when the glass is broken.

7.5 Absolute Maximum Ratings and Power Protection Circuit

7.5.1 Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.
7.5.2 Please do not leave LCD module in the environment of high humidity and high temperature for a long time.
7.5.3 It's recommended employing protection circuit for power supply.
7.6 Operation
7.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.
7.6.2 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.
7.6.3 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.
7.6.4 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

7.7 Static Electricity

7.7.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.
7.7.2 Because LCD module uses CMOS-IC on TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge.
7.7.3 Persons who handle the module should be grounded through adequate methods.

7.8 Disposal

When disposing LCD module, obey the local environmental regulations.

7.9 OTHERS

7.9.1 A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight land strong UV rays.
7.9.2 Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
7.9.3 For the packaging box, please pay attention to the followings:
7.9.3.1 Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.
7.9.3.2 Please do not pile them up more than 6 boxes. (They are not designed so.) And please do not turn over.
7.9.3.3 Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
7.9.3.4 Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)